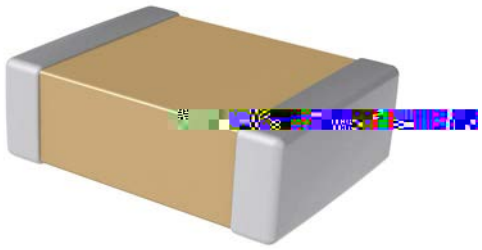
Overview

KEMET's U2J dielectric features a maximum operating temperature of 125°C and is considered stable. The Electronics Industries Alliance (EIA) characterizes U2J dielectric as a Class I material. Components of this classification are temperature compensating and are suited for resonant circuit applications or those where Q and stability of capacitance characteristics are required. U2J is an extremely stable dielectric material that exhibits a negligible shift in capacitance with respect to voltage and boasts a predictable and linear change in capacitance with reference to ambient temperature with no aging effect. In addition, U2J dielectric extends the available capacitance range of Class I MLCCs to achieve values previously only available using Class II dielectric materials like X7R, X5R, Y5V and Z5U. U2J is not sensitive to DC Bias as compared to Class II dielectric materials and retains over 99% of nominal capacitance at full rated voltage. Capacitance change is limited to −750 ± 120 ppm /°C from −55°C to +125°C. These devices are Lead-free, RoHS and REACH compliant without exception and are capable of withstanding multiple passes through a Lead-free solder reflow profile.

Benefits

- Low dissipation factor DF < 0.1%
- Low noise solution similar to C0G
- Low ESR and ESL
- High thermal stability
- High ripple current capability
- Preferred capacitance solution at line frequencies and into the MHz range
- R3VHIVMRK-RJSVQEXMSR



Click image above for interactive 3D content

Open PDF in Adobe Reader for full functionality

'		'		J	3	J	A	C	TU
Ceramic	Case Size (L" x W")	Specification/ Series[1]	Capacitance Code (pF)	Capacitance Tolerance[2]	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Termination Finish[3]	Packaging/ Grade (C-Spec)
	0402 0603 0805 1206 1210 1812	C = Standard	Two significant digits + number of zeros.	F = ±1% G = ±2% J = ±5% K = ±10% M = ±20%	8 = 10 4 = 16 3 = 25 5 = 50	J = U2J	A = N/A	C = 100% Matte Sn	See "Packaging C-Spec Ordering Options Table" below

[1] Flexible termination option is available. Please see FT-CAP product bulletin C1062_C0G_FT-CAP_SMD

[2] Additional capacitance tolerance offerings may be available. Contact KEMET for details.

Packaging C-Spec Ordering Options Table

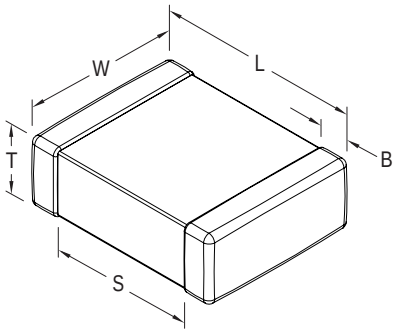
Packaging Type[1]	Packaging/Grade Ordering Code (C-Spec)
Bulk Bag/Unmarked	Not required (Blank)
7" Reel/Unmarked	TU
13" Reel/Unmarked	7411 (EIA 0603 and smaller case sizes) 7210 (EIA 0805 and larger case sizes)
7" Reel/Unmarked/2 mm pitch[2]	7081
13" Reel/Unmarked/2 mm pitch[2]	7082

[1] Default packaging is "Bulk Bag". An ordering code C-Spec is not required for "Bulk Bag" packaging.

[1] The terms "Marked" and "Unmarked" pertain to laser marking option of capacitors. All packaging options labeled as "Unmarked" will contain capacitors that have not been laser marked. The option to laser mark is not available on these devices. For more information see "Capacitor Marking".

[2]

Dimensions – Millimeters (Inches)



EIA Size Code	Metric Size Code	**L** Length	**W** Width	**T** Thickness	**B** Bandwidth	S Separation Minimum	Mounting Technique
0402	1005	1.00 (0.040)±0.05 (0.002)	0.50 (0.020)± 0.05 (0.002)	See Table 2 for Thickness	0.30 (0.012)±0.10 (0.004)	0.30 (0.012)	Solder reflow only
0603	1608	1.60 (0.063)±0.15 (0.006)	0.80 (0.032)±0.15 (0.006)		0.35 (0.014)±0.15 (0.006)	0.70 (0.028)	Solder wave or Solder reflow
0805	2012	2.00 (0.079)±0.20 (0.008)	1.25 (0.049)±0.20 (0.008)		0.50 (0.02)±0.25 (0.010)	0.75 (0.030)	
1206	3216	3.20 (0.126)±0.20 (0.008)	1.60 (0.063)±0.20 (0.008)		0.50 (0.02)±0.25 (0.010)	N/A	
1210	3225	3.20 (0.126)±0.20 (0.008)	2.50 (0.098)±0.20 (0.008)		0.50 (0.02)±0.25 (0.010)		Solder reflow only
1812	4532	4.50 (0.177)±0.30 (0.012)	3.20 (0.126)±0.30 (0.012)		0.60 (0.024)±0.35 (0.014)		

Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	−55°C to +125°C
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	−750±120 ppm/°C
Aging Rate (Maximum % Capacitance Loss/Decade Hour)	0.1%
Dielectric Withstanding Voltage (DWV)	250% of rated voltage (5±1 seconds and charge/discharge not exceeding 50 mA)
Dissipation Factor (DF) Maximum Limit at 25°C	0.1%
Insulation Resistance (IR) Limit at 25°C	1,000 megohm microfarads or 100 GΩ (Rated voltage applied for 120±5 seconds at 25°C)

To obtain IR limit, divide MΩ-µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.
Capacitance and dissipation factor (DF) measured under the following conditions:

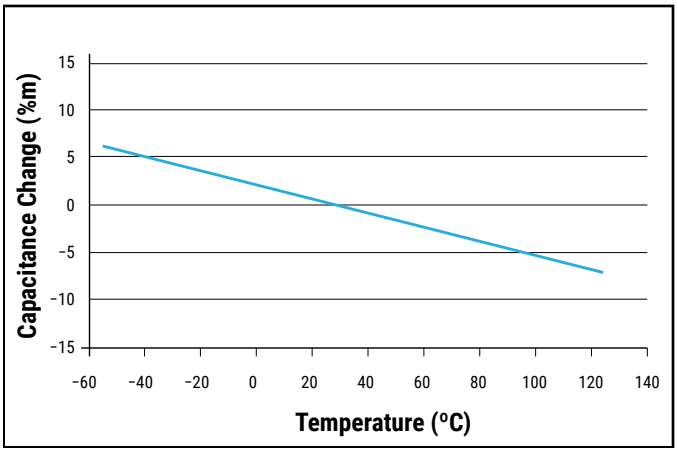
1 MHz ±100 kHz and 1.0 Vrms ±0.2 V if capacitance ≤ 1,000 pF

1 kHz ±50 Hz and 1.0 Vrms ±0.2 V if capacitance > 1,000 pF

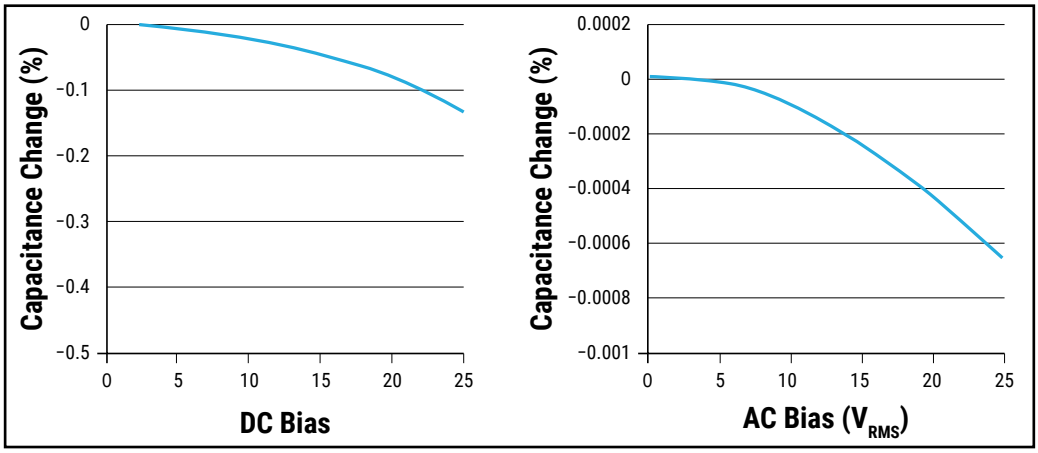
Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

Electrical Characteristics (Typical)

Capacitance vs. Temperature (TCC)



DC & AC Bias Effective Capacitance



Post Environmental Limits

High Temperature Life, Biased Humidity, Moisture Resistance					
Dielectric	Rated DC Voltage	Capacitance Value	Dissipation Factor (Maximum %)	Capacitance Shift	Insulation Resistance
U2J	All	All	0.5	0.3% or ±0.25 pF	10% of Initial Limit

Table 1A – Capacitance Range/Selection Waterfall (0402 – 1812 Case Sizes)

Table 1A – Capacitance Range/Selection Waterfall (0402 – 1812 Case Sizes) cont'd

Capacitance	Cap Code	Case Size/ Series	C0402C				C0603C				C0805C				C1206C				C1210C				C1812C			
		Voltage Code	8	4	**3**	5	8	4	**3**	5	8	4	**3**	5	8	4	**3**	5	8	4	**3**	5	8	4	**3**	5
		Rated Voltage (VDC)	10	16	25	50	10	16	25	50	10	16	25	50	10	16	25	50	10	16	25	50	10	16	25	50
		Capacitance Tolerance	Product Availability and Chip Thickness Codes See Table 2 for Chip Thickness Dimensions																							
15,000 pF	153	F G J K M					CF	CF	CF		DN	DN	DN	DN	EB	EB	EB	EB	FB	FB	FB	FB	GB	GB	GB	
18,000 pF	183	F G J K M									DN	DN	DN	DN	EB	EB	EB	EB	FB	FB	FB	FB	GB	GB	GB	
22,000 pF	223	F G J K M									DN	DN	DN	DP	EB	EB	EB	EB	FB	FB	FB	FB	GB	GB	GB	
27,000 pF	273	F G J K M									DP	DP	DP	DP	EB	EB	EB	EB	FB	FB	FB	FB	GB	GB	GB	
33,000 pF	333	F G J K M									DP	DP	DP	DG	EB	EB	EB	EB	FB	FB	FB	FB	GB	GB	GB	
47,000 pF	393	F G J K M									DG	DG	DG	DG	EB	EB	EB	EB	FB	FB	FB	FB	GB	GB	GB	
47,000 pF	473	F G J K M									DG	DG	DG	DG	EB	EB	EB	EB	FB	FB	FB	FB	GB	GB	GB	
56,000 pF	563	F G J K M									DG	DG	DG		EB	EB	EB	EC	FB	FB	FB	FB	GB	GB	GB	
68,000 pF	683	F G J K M													EC	EC	EC	EC	FB	FB	FB	FB	GB	GB	GB	
82,000 pF	823	F G J K M													EC	EC	EC	EE	FB	FB	FB	FB	GB	GB	GB	
100,000 pF	104	F G J K M													EC	EC	EC	EF	FB	FB	FB	FC	GB	GB	GB	
120,000 pF	124	F G J K M													EF	EF	EF	EH	FC	FC	FC	FE	GB	GB	GB	
150,000 pF	154	F G J K M													EF	EF	EF	EH	FE	FE	FE	FG	GB	GB	GB	
180,000 pF	184	F G J K M													EH	EH	EH		FG	FG	FG	FG	GB	GB	GB	
220,000 pF	224	F G J K M													EH	EH	EH		FG	FG	FG	FH	GB	GB	GB	
270,000 pF	274	F G J K M																	FH	FH	FH	FM	GB	GB	GB	
330,000 pF	334	F G J K M																	FM	FM	FM		GC	GC	GC	
390,000 pF	394	F G J K M																					GH	GH	GH	
470,000 pF	474	F G J K M																					GK	GK	GK	
		Rated Voltage (VDC)	10	16	25	50	10	16	25	50	10	16	25	50	10	16	25	50	10	16	25	50	10	16	25	50
Capacitance	Cap Code	Voltage Code	8	4	**3**	5	8	4	**3**	5	8	4	**3**	5	8	4	**3**	5	8	4	**3**	5	8	4	**3**	5
		Case Size/Series	C0402C				C0603C				C0805C				C1206C				C1210C				C1812C			

Table 2A – Chip Thickness/Tape & Reel Packaging Quantities

Thickness Code	Case Size[1]	Thickness ± Range (mm)	Paper Quantity[1]		Plastic Quantity	
			7" Reel	13" Reel	7" Reel	13" Reel
BB	0402	0.50 ± 0.05	10,000	50,000	0	0
CF	0603	0.80 ± 0.07*	4,000	15,000	0	0
DN	0805	0.78 ± 0.10*	4,000	15,000	0	0
DP	0805	0.90 ± 0.10*	4,000	15,000	0	0
DG	0805	1.25 ± 0.15	0	0	2,500	10,000
EB	1206	0.78 ± 0.10	4,000	10,000	4,000	10,000
EC	1206	0.90 ± 0.10	0	0	4,000	10,000
EE	1206	1.10 ± 0.10	0	0	2,500	10,000
EF	1206	1.20 ± 0.15	0	0	2,500	10,000
EH	1206	1.60 ± 0.20	0	0	2,000	8,000
FB	1210	0.78 ± 0.10	0	0	4,000	10,000
FC	1210	0.90 ± 0.10	0	0	4,000	10,000
FE	1210	1.00 ± 0.10	0	0	2,500	10,000
FG	1210	1.25 ± 0.15	0	0	2,500	10,000
FH	1210	1.55 ± 0.15	0	0	2,000	8,000
FM	1210	1.70 ± 0.20	0	0	2,000	8,000
GB	1812	1.00 ± 0.10	0	0	1,000	4,000
GC	1812	1.10 ± 0.10	0	0	1,000	4,000
GH	1812	1.40 ± 0.15	0	0	1,000	4,000
GK	1812	1.60 ± 0.20	0	0	1,000	4,000
Thickness Code	Case Size[1]	Thickness ± Range (mm)	7" Reel	13" Reel	7" Reel	13" Reel
			Paper Quantity[1]		Plastic Quantity	

Package quantity based on finished chip thickness specifications.
[1] If ordering using the 2 mm Tape and Reel pitch option, the packaging quantity outlined in the table above will be doubled. This option is limited to EIA 0603 (1608 metric) case size devices. For more information regarding 2 mm pitch option see "Tape & Reel Packaging Information".

Table 2B – Bulk Packaging Quantities

Packaging Type		Loose Packaging	
		Bulk Bag (default)	
Packaging C-Spec[1]		N/A[2]	
Case Size		Packaging Quantities (pieces/unit packaging)	
EIA (in)	Metric (mm)	Minimum	Maximum
0402	1005	1	50,000
0603	1608		
0805	2012		
1206	3216		
1210	3225		
1812	4532		20,000

[1] The "Packaging C-Spec" is a 4 to 8 digit code which identifies the packaging type and/or product grade. When ordering, the proper code must be included in the 15th through 22nd character positions of the ordering code. See "Ordering Information" section of this document for further details. Commercial Grade product ordered without a packaging C-Spec will default to our standard "Bulk Bag" packaging. Contact KEMET if you require a bulk bag packaging option for Automotive Grade products.
[2] A packaging C-Spec (see note 1 above) is not required for "Bulk Bag" packaging (excluding Anti-Static Bulk Bag and Automotive Grade products). The 15th through 22nd character positions of the ordering code should be left blank. All product ordered without a packaging C-Spec will default to our standard "Bulk Bag" packaging.

Table 3 – Chip Capacitor Land Pattern Design Recommendations per IPC–7351

EIA Size Code	Metric Size Code	Density Level A: Maximum (Most) Land Protrusion (mm)					Density Level B: Median (Nominal) Land Protrusion (mm)					Density Level C: Minimum (Least) Land Protrusion (mm)				
		C	**Y**	**X**	V1	V2	C	**Y**	**X**	V1	V2	C	**Y**	**X**	V1	V2
0402	1005	0.50	0.72	0.72	2.20	1.20	0.45	0.62	0.62	1.90	1.00	0.40	0.52	0.52	1.60	0.80
0603	1608	0.90	1.15	1.10	4.00	2.10	0.80	0.95	1.00	3.10	1.50	0.60	0.75	0.90	2.40	1.20
0805	2012	1.00	1.35	1.55	4.40	2.60	0.90	1.15	1.45	3.50	2.00	0.75	0.95	1.35	2.80	1.70
1206	3216	1.60	1.35	1.90	5.60	2.90	1.50	1.15	1.80	4.70	2.30	1.40	0.95	1.70	4.00	2.00
1210	3225	1.60	1.35	2.80	5.65	3.80	1.50	1.15	2.70	4.70	3.20	1.40	0.95	2.60	4.00	2.90
1210[1]	3225	1.50	1.60	2.90	5.60	3.90	1.40	1.40	2.80	4.70	3.30	1.30	1.20	2.70	4.00	3.00
1812	4532	2.15	1.60	3.60	6.90	4.60	2.05	1.40	3.50	6.00	4.00	1.95	1.20	3.40	5.30	3.70

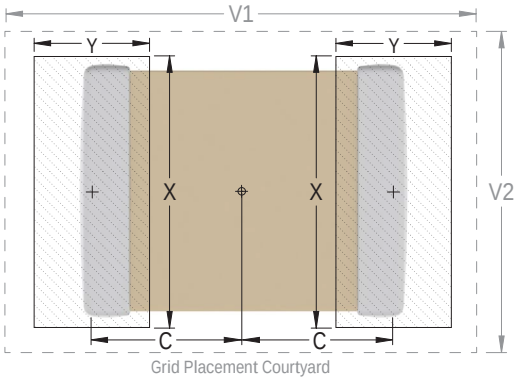
[1] *Only for capacitance values ≥ 22 µF*

Density Level A: *For low-density product applications. Recommended for wave solder applications and provides a wider process window for reflow solder processes. KEMET only recommends wave soldering of EIA 0603, 0805 and 1206 case sizes.*

Density Level B: *For products with a moderate level of component density. Provides a robust solder attachment condition for reflow solder processes.*

Density Level C: *For high component density product applications. Before adapting the minimum land pattern variations the user should perform qualification testing based on the conditions outlined in IPC Standard 7351 (IPC–7351).*

Image below based on Density Level B for an EIA 1210 case size.



Soldering Process

Recommended Soldering Technique:

- Solder wave or solder reflow for EIA case sizes 0603, 0805 and 1206
- All other EIA case sizes are limited to solder reflow only

Recommended Reflow Soldering Profile:

KEMET's families of surface mount multilayer ceramic capacitors (SMD MLCCs) are compatible with wave (single or dual), convection, IR or vapor phase reflow techniques. Preheating of these components is recommended to avoid extreme thermal stress. KEMET's recommended profile conditions for convection and IR reflow reflect the profile conditions of the IPC/J-STD-020 standard for moisture sensitivity testing. These devices can safely withstand a maximum of three reflow passes at these conditions.

Profile Feature	Termination Finish	
	SnPb	100% Matte Sn
Preheat/Soak		
Temperature Minimum (T_{Smin})	100°C	150°C
Temperature Maximum (T_{Smax})	150°C	200°C
Time (t_S) from T_{Smin} to T_{Smax}	60 – 120 seconds	60 – 120 seconds
Ramp-Up Rate (T_L to T_P)	3°C/second maximum	3°C/second maximum
Liquidous Temperature (T_L)	183°C	217°C
Time Above Liquidous (t_L)	60 – 150 seconds	60 – 150 seconds
Peak Temperature (T_P)	235°C	260°C
Time Within 5°C of Maximum Peak Temperature (t_P)	20 seconds maximum	30 seconds maximum
Ramp-Down Rate (T_P to T_L)	6°C/second maximum	6°C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

Note 1: All temperatures refer to the center of the package, measured on the capacitor body surface that is facing up during assembly reflow.

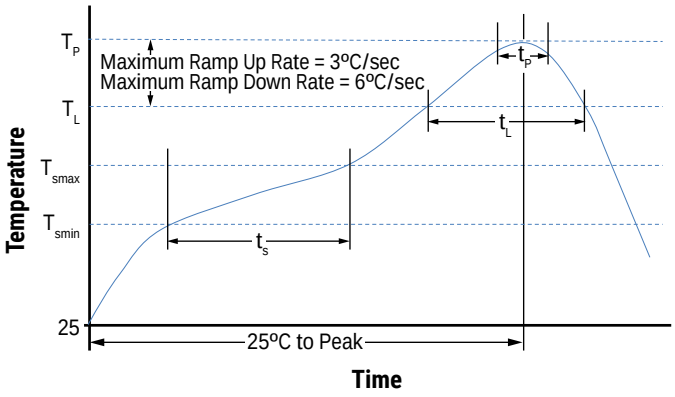


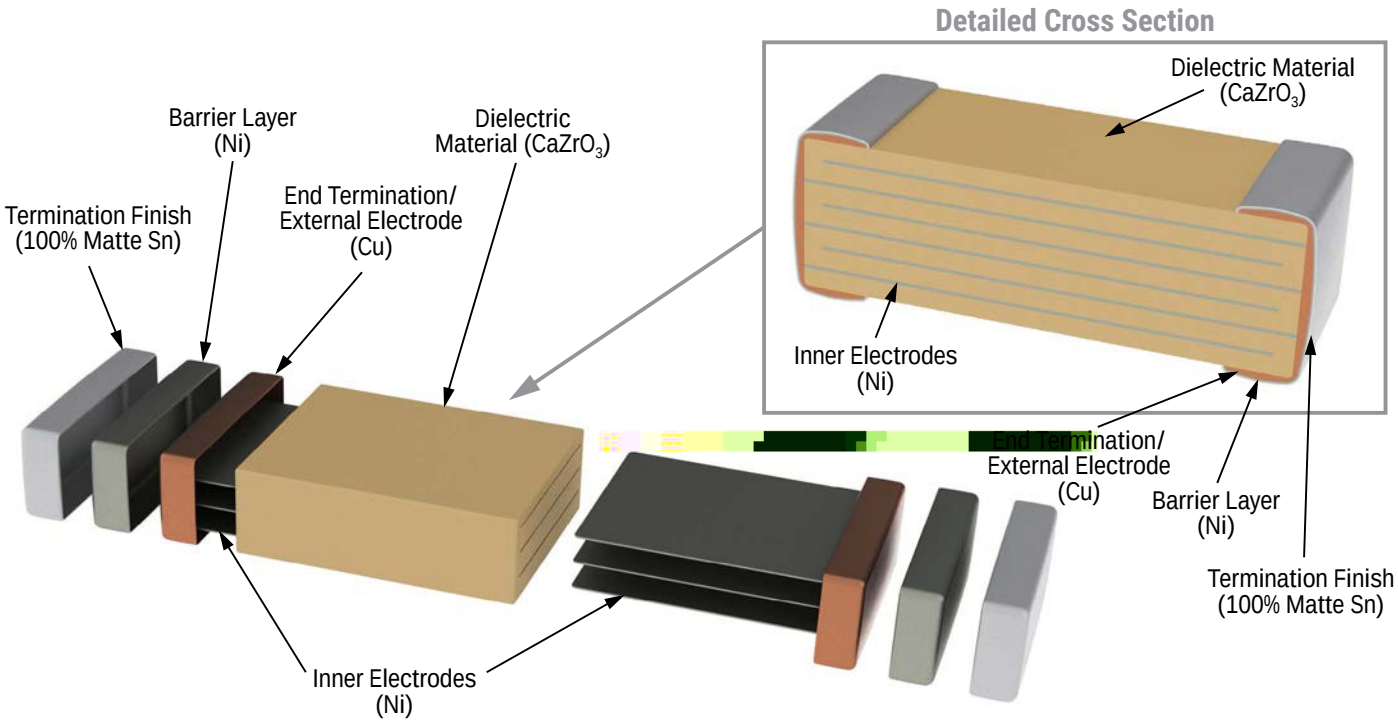
Table 4 – Performance & Reliability: Test Methods and Conditions

<table>
<tr><th>Stress</th><th>Reference</th><th>Test or Inspection Method</th></tr>
<tr><td>Terminal Strength</td><td>JIS–C–6429</td><td>Appendix 1, Note:
<table>
<tr><th>Package Size (L" x W")</th><th>Force</th><th>Duration</th></tr>
<tr><td>0402</td><td>5 N (0.51 kg)</td><td rowspan="3">60 seconds</td></tr>
<tr><td>0603</td><td>10 N (1.02 kg)</td></tr>
<tr><td>≥ 0805</td><td>18 N (1.83 kg)</td></tr>
</table></td></tr>
<tr><td>Board Flex</td><td>JIS–C–6429</td><td>Appendix 2, Note: 3.0 mm (minimum).</td></tr>
<tr><td rowspan="4">Solderability</td><td rowspan="4">J–STD–002</td><td>Magnification 50 X Conditions:</td></tr>
<tr><td>a) Method B, 4 hours at 155°C, dry heat at 235°C</td></tr>
<tr><td>b) Method B at 215°C category 3</td></tr>
<tr><td>c) Method D, category 3 at 260°C</td></tr>
<tr><td>Temperature Cycling</td><td>JESD22 Method JA-104</td><td>1,000 cycles (–55°C to +125°C). Measurement at 24 hours +/– 4 hours after test conclusion.</td></tr>
<tr><td rowspan="2">Biased Humidity</td><td rowspan="2">MIL-STD-202 Method 103</td><td>Load Humidity: 1,000 hours 85°C/85% RH and rated voltage. Add 100 K ohm resistor. Measurement at 24 hours +/– 4 hours after test conclusion.</td></tr>
<tr><td>Low Volt Humidity: 1,000 hours 85C°/85% RH and 1.5 V. Add 100 K ohm resistor. Measurement at 24 hours +/– 4 hours after test conclusion.</td></tr>
<tr><td>Moisture Resistance</td><td>MIL-STD-202 Method 106</td><td>t = 24 hours/cycle. Steps 7a & 7b not required. Measurement at 24 hrs. +/– 4 hours after test conclusion.</td></tr>
<tr><td>Thermal Shock</td><td>MIL-STD-202 Method 107</td><td>–55°C/+125°C. Note: Number of cycles required – 300. Maximum transfer time – 20 seconds. Dwell time – 15 minutes. Air – Air.</td></tr>
<tr><td>High Temperature Life</td><td>MIL-STD-202
Method 108/EIA -198</td><td>1,000 hours at 125°C with 2 X rated voltage applied.</td></tr>
<tr><td>Storage Life</td><td>MIL-STD-202 Method 108</td><td>125°C, 0 VDC for 1,000 hours.</td></tr>
<tr><td>Vibration</td><td>MIL-STD-202 Method 204</td><td>5 G's for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8" X 5" PCB 0.031" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10 – 2,000 Hz</td></tr>
<tr><td>Mechanical Shock</td><td>MIL-STD-202 Method 213</td><td>Figure 1 of Method 213, Condition F.</td></tr>
<tr><td>Resistance to Solvents</td><td>MIL-STD-202 Method 215</td><td>Add aqueous wash chemical, OKEM clean or equivalent.</td></tr>
</table>

Storage and Handling

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature–reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. Temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within 1.5 years of receipt.

Construction



Capacitor Marking (Optional):

Laser marking option is not available on:

- C0G, U2J, Ultra Stable X8R, and Y5V dielectric devices
- EIA 0402 case size devices
- EIA 0603 case size devices with Flexible Termination option.
- KPS Commercial and Automotive grade stacked devices.

These capacitors are supplied unmarked only.

Figure 1 – Embossed (Plastic) Carrier Tape Dimensions

Figure 2 – Punched (Paper) Carrier Tape Dimensions

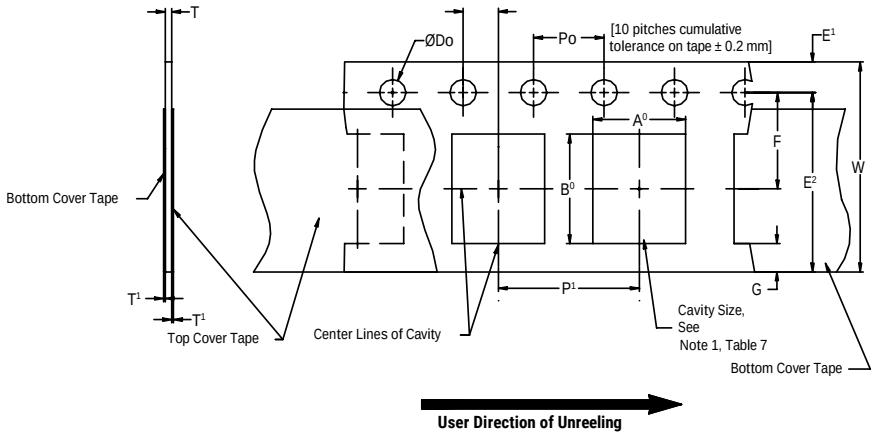


Table 7 – Punched (Paper) Carrier Tape Dimensions

Metric will govern

Constant Dimensions — Millimeters (Inches)							
Tape Size	D_0	E_1	P_0	P_2	T_1 Maximum	G Minimum	R Reference Note 2
8 mm	1.5 +0.10 -0.0 (0.059 +0.004 -0.0)	1.75 ±0.10 (0.069 ±0.004)	4.0 ±0.10 (0.157 ±0.004)	2.0 ±0.05 (0.079 ±0.002)	0.10 (0.004) Maximum	0.75 (0.030)	25 (0.984)

Variable Dimensions — Millimeters (Inches)							
Tape Size	Pitch	E2 Minimum	F	P_1	T Maximum	W Maximum	$A_0 B_0$
8 mm	Half (2 mm)	6.25 (0.246)	3.5 ±0.05 (0.138 ±0.002)	2.0 ±0.05 (0.079 ±0.002)	1.1 (0.098)	8.3 (0.327)	Note 1
8 mm	Single (4 mm)			4.0 ±0.10 (0.157 ±0.004)		8.3 (0.327)	

1. The cavity defined by A_0, B_0 and T shall surround the component with sufficient clearance that:
a) the component does not protrude beyond either surface of the carrier tape.
b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.
c) rotation of the component is limited to 20° maximum (see Figure 3).
d) lateral movement of the component is restricted to 0.5 mm maximum (see Figure 4).
e) see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.
2. The tape with or without components shall pass around R without damage (see Figure 6).

Packaging Information Performance Notes

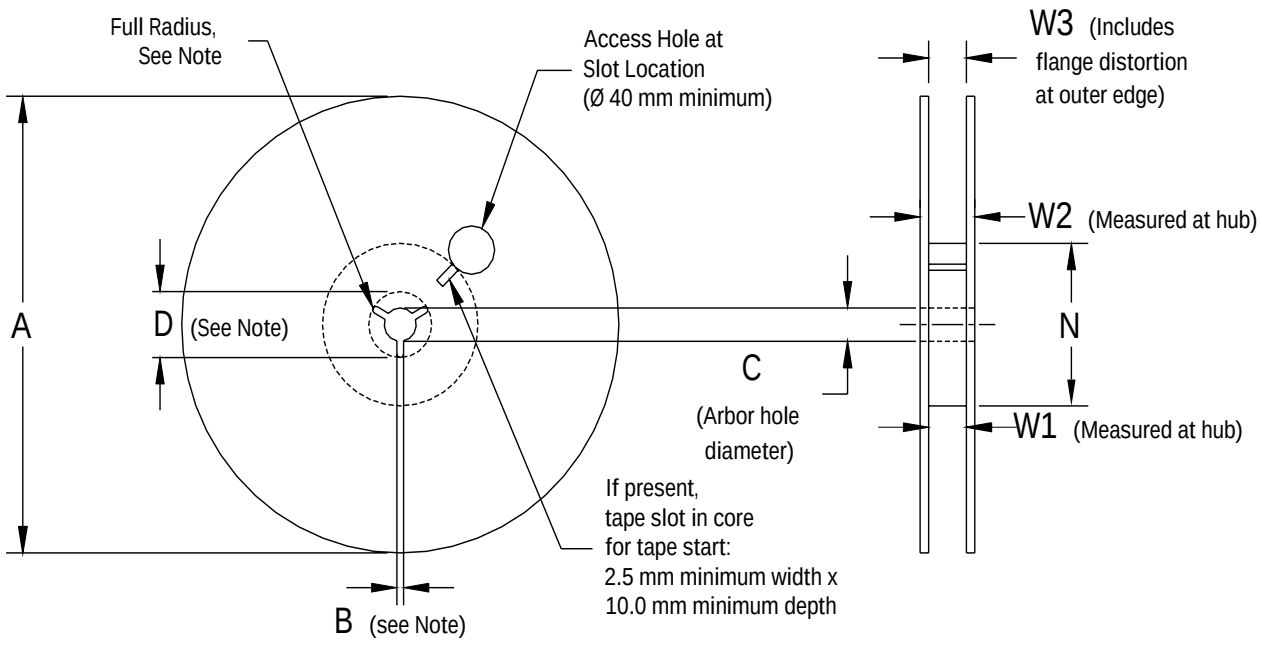
1. Cover Tape Break Force: 1.0 Kg minimum.
2. Cover Tape Peel Strength: The total peel strength of the cover tape from the carrier tape shall be:

Tape Width	Peel Strength
8 mm	0.1 to 1.0 Newton (10 to 100 gf)
12 and 16 mm	0.1 to 1.3 Newton (10 to 130 gf)

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300 ±10 mm/minute.
3. Labeling: Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. *Refer to EIA Standards 556 and 624*.

Figure 3 – Maximum Component Rotation

Figure 6 – Reel Dimensions



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Table 8 – Reel Dimensions

Metric will govern

Constant Dimensions — Millimeters (Inches)				
Tape Size	A	B Minimum	C	D Minimum
8 mm	178 ±0.20 (7.008 ±0.008) or 330 ±0.20 (13.000 ±0.008)	1.5 (0.059)	13.0 +0.5/-0.2 (0.521 +0.02/-0.008)	20.2 (0.795)
12 mm				
16 mm				

Variable Dimensions — Millimeters (Inches)				
Tape Size	N Minimum	W_1	W_2 Maximum	W_3
8 mm	50 (1.969)	8.4 +1.5/-0.0 (0.331 +0.059/-0.0)	14.4 (0.567)	Shall accommodate tape width without interference
12 mm		12.4 +2.0/-0.0 (0.488 +0.078/-0.0)	18.4 (0.724)	
16 mm		16.4 +2.0/-0.0 (0.646 +0.078/-0.0)	22.4 (0.882)	

Figure 7 – Tape Leader & Trailer Dimensions

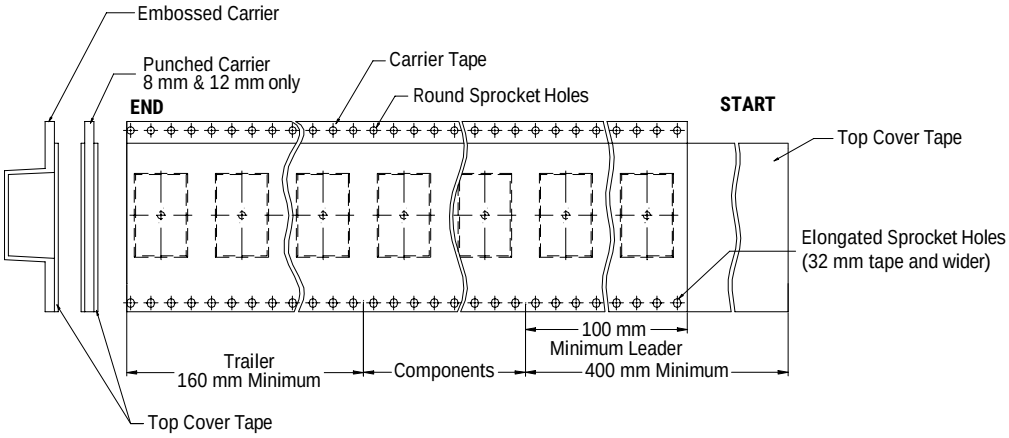
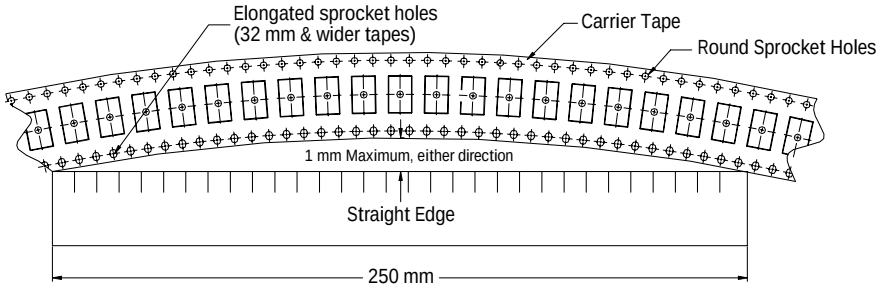


Figure 8 – Maximum Camber



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