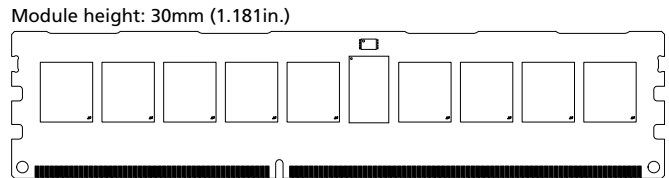


# DDR3 SDRAM RDIMM

**MT18JSF25672PDZ – 2GB**
**MT18JSF51272PDZ – 4GB**

## Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC3-14900, PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 2GB (256 Meg x 72), 4GB (512 Meg x 72)
- $V_{DD} = 1.5V \pm 0.075V$
- $V_{DDSPD} = 3.0\text{--}3.6V$
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual rank
- On-board I<sup>2</sup>C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

**Figure 1: 240-Pin RDIMM (MO-269 R/C B1)**


## Options

- Operating temperature
  - Commercial ( $0^{\circ}C \leq T_A \leq +70^{\circ}C$ )
- Package
  - 240-pin DIMM (halogen-free)
- Frequency/CAS latency
  - 1.07ns @ CL = 13 (DDR3-1866)
  - 1.25ns @ CL = 11 (DDR3-1600)
  - 1.5ns @ CL = 9 (DDR3-1333)
  - 1.87ns @ CL = 7 (DDR3-1066)

## Marking

None  
Z  
-1G9  
-1G6  
-1G4  
-1G1

**Table 1: Key Timing Parameters**

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								t <sub>RCD</sub> (ns)	t <sub>RP</sub> (ns)	t <sub>RC</sub> (ns)
		CL = 13	CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G9	PC3-14900	1866	1600	1333	1333	1066	1066	800	667	13.125	13.125	47.125
-1G6	PC3-12800	–	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	–	800	667	15	15	52.5



**Table 2: Addressing**

Parameter	2GB	4GB
Refresh count	8K	8K
Row address	16K A[13:0]	32K A[14:0]
Device bank address	8 BA[2:0]	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)	2Gb (256 Meg x 8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	2 S#[1:0]	2 S#[1:0]

**Table 3: Part Numbers and Timing Parameters – 2GB Modules**

Base device: MT41J128M8,<sup>1</sup> 1Gb DDR3 SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MT18JSF25672PDZ-1G9__	2GB	256 Meg x 72	14.9 GB/s	1.07ns/1866 MT/s	13-13-13
MT18JSF25672PDZ-1G6__	2GB	256 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT18JSF25672PDZ-1G4__	2GB	256 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT18JSF25672PDZ-1G1__	2GB	256 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

**Table 4: Part Numbers and Timing Parameters – 4GB Modules**

Base device: MT41J256M8,<sup>1</sup> 2Gb DDR3 SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- <sup>t</sup> RCD- <sup>t</sup> RP)
MT18JSF51272PDZ-1G9__	4GB	512 Meg x 72	14.9 GB/s	1.07ns/1866 MT/s	13-13-13
MT18JSF51272PDZ-1G6__	4GB	512 Meg x 72	12.8 GB/s	1.25ns/1600 MT/s	11-11-11
MT18JSF51272PDZ-1G4__	4GB	512 Meg x 72	10.6 GB/s	1.5ns/1333 MT/s	9-9-9
MT18JSF51272PDZ-1G1__	4GB	512 Meg x 72	8.5 GB/s	1.87ns/1066 MT/s	7-7-7

- Notes:
1. The data sheet for the base device can be found on Micron’s Web site.
  2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT18JSF51272PDZ-1G6K1.



## Pin Assignments

Table 5: Pin Assignments

240-Pin DDR3 RDIMM Front								240-Pin DDR3 RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V <sub>REFDQ</sub>	31	DQ25	61	A2	91	DQ41	121	V <sub>SS</sub>	151	V <sub>SS</sub>	181	A1	211	V <sub>SS</sub>
2	V <sub>SS</sub>	32	V <sub>SS</sub>	62	V <sub>DD</sub>	92	V <sub>SS</sub>	122	DQ4	152	DM3/ TDQS12	182	V <sub>DD</sub>	212	DM5/ TDQS14
3	DQ0	33	DQS3#	63	NF	93	DQS5#	123	DQ5	153	NF/ TDQS12#	183	V <sub>DD</sub>	213	NF/ TDQS14#
4	DQ1	34	DQS3	64	NF	94	DQS5	124	V <sub>SS</sub>	154	V <sub>SS</sub>	184	CK0	214	V <sub>SS</sub>
5	V <sub>SS</sub>	35	V <sub>SS</sub>	65	V <sub>DD</sub>	95	V <sub>SS</sub>	125	DM0/ TDQS9	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	V <sub>DD</sub>	96	DQ42	126	NF/ TDQS9#	156	DQ31	186	V <sub>DD</sub>	216	DQ47
7	DQS0	37	DQ27	67	V <sub>REFCA</sub>	97	DQ43	127	V <sub>SS</sub>	157	V <sub>SS</sub>	187	EVENT#	217	V <sub>SS</sub>
8	V <sub>SS</sub>	38	V <sub>SS</sub>	68	Par_In	98	V <sub>SS</sub>	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	V <sub>DD</sub>	99	DQ48	129	DQ7	159	CB5	189	V <sub>DD</sub>	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	V <sub>SS</sub>	160	V <sub>SS</sub>	190	BA1	220	V <sub>SS</sub>
11	V <sub>SS</sub>	41	V <sub>SS</sub>	71	BA0	101	V <sub>SS</sub>	131	DQ12	161	DM8/ TDQS17	191	V <sub>DD</sub>	221	DM6/ TDQS15
12	DQ8	42	DQS8#	72	V <sub>DD</sub>	102	DQS6#	132	DQ13	162	NF/ TDQS17#	192	RAS#	222	NF/ TDQS15#
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	V <sub>SS</sub>	163	V <sub>SS</sub>	193	S0#	223	V <sub>SS</sub>
14	V <sub>SS</sub>	44	V <sub>SS</sub>	74	CAS#	104	V <sub>SS</sub>	134	DM1/ TDQS10	164	CB6	194	V <sub>DD</sub>	224	DQ54
15	DQS1#	45	CB2	75	V <sub>DD</sub>	105	DQ50	135	NF/ TDQS10#	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	S1#	106	DQ51	136	V <sub>SS</sub>	166	V <sub>SS</sub>	196	A13	226	V <sub>SS</sub>
17	V <sub>SS</sub>	47	V <sub>SS</sub>	77	ODT1	107	V <sub>SS</sub>	137	DQ14	167	NC	197	V <sub>DD</sub>	227	DQ60
18	DQ10	48	V <sub>TT</sub>	78	V <sub>DD</sub>	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	V <sub>TT</sub>	79	NC	109	DQ57	139	V <sub>SS</sub>	169	CKE1	199	V <sub>SS</sub>	229	V <sub>SS</sub>
20	V <sub>SS</sub>	50	CKE0	80	V <sub>SS</sub>	110	V <sub>SS</sub>	140	DQ20	170	V <sub>DD</sub>	200	DQ36	230	DM7/ TDQS16
21	DQ16	51	V <sub>DD</sub>	81	DQ32	111	DQS7#	141	DQ21	171	A15	201	DQ37	231	NF/ TDQS16#
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V <sub>SS</sub>	172	A14	202	V <sub>SS</sub>	232	V <sub>SS</sub>
23	V <sub>SS</sub>	53	Err_Out#	83	V <sub>SS</sub>	113	V <sub>SS</sub>	143	DM2/ TDQS11	173	V <sub>DD</sub>	203	DM4/ TDQS13	233	DQ62
24	DQS2#	54	V <sub>DD</sub>	84	DQS4#	114	DQ58	144	NF/ TDQS11#	174	A12	204	NF/ TDQS13#	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V <sub>SS</sub>	175	A9	205	V <sub>SS</sub>	235	V <sub>SS</sub>
26	V <sub>SS</sub>	56	A7	86	V <sub>SS</sub>	116	V <sub>SS</sub>	146	DQ22	176	V <sub>DD</sub>	206	DQ38	236	V <sub>DDSPD</sub>
27	DQ18	57	V <sub>DD</sub>	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V <sub>SS</sub>	178	A6	208	V <sub>SS</sub>	238	SDA
29	V <sub>SS</sub>	59	A4	89	V <sub>SS</sub>	119	SA2	149	DQ28	179	V <sub>DD</sub>	209	DQ44	239	V <sub>SS</sub>
30	DQ24	60	V <sub>DD</sub>	90	DQ40	120	V <sub>TT</sub>	150	DQ29	180	A3	210	DQ45	240	V <sub>TT</sub>

## Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

**Table 6: Pin Descriptions**

Symbol	Type	Description
Ax	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	<b>Bank address inputs:</b> Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	<b>Clock:</b> Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	<b>Clock enable:</b> Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	<b>Data mask (x8 devices only):</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	<b>On-die termination:</b> Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	<b>Parity input:</b> Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	<b>Reset:</b> RESET# is an active LOW asynchronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	<b>Chip select:</b> Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	<b>Serial address inputs:</b> Used to configure the temperature sensor/SPD EEPROM address range on the I <sup>2</sup> C bus.
SCL	Input	<b>Serial clock for temperature sensor/SPD EEPROM:</b> Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I <sup>2</sup> C bus.
CBx	I/O	<b>Check bits:</b> Used for system error detection and correction.
DQx	I/O	<b>Data input/output:</b> Bidirectional data bus.
DQSx, DQSx#	I/O	<b>Data strobe:</b> Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

**Table 6: Pin Descriptions (Continued)**

Symbol	Type	Description
SDA	I/O	<b>Serial data:</b> Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I <sup>2</sup> C bus.
TDQSx, TDQSx#	Output	<b>Redundant data strobe (x8 devices only):</b> TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	<b>Parity error output:</b> Parity error found on the command and address bus.
EVENT#	Output (open drain)	<b>Temperature event:</b> The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V <sub>DD</sub>	Supply	<b>Power supply:</b> 1.5V ±0.075V. The component V <sub>DD</sub> and V <sub>DDQ</sub> are connected to the module V <sub>DD</sub> .
V <sub>DDSPD</sub>	Supply	<b>Temperature sensor/SPD EEPROM power supply:</b> 3.0–3.6V.
V <sub>REFCA</sub>	Supply	<b>Reference voltage:</b> Control, command, and address V <sub>DD</sub> /2.
V <sub>REFDQ</sub>	Supply	<b>Reference voltage:</b> DQ, DM V <sub>DD</sub> /2.
V <sub>SS</sub>	Supply	Ground.
V <sub>TT</sub>	Supply	<b>Termination voltage:</b> Used for control, command, and address V <sub>DD</sub> /2.
NC	–	<b>No connect:</b> These pins are not connected on the module.
NF	–	<b>No function:</b> These pins are connected within the module, but provide no functionality.



## DQ Map

Table 7: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U2	0	2	9	U3	0	10	18
	1	5	123		1	13	132
	2	7	129		2	15	138
	3	0	3		3	8	12
	4	6	128		4	14	137
	5	4	122		5	12	131
	6	3	10		6	11	19
	7	1	4		7	9	13
U4	0	18	27	U5	0	26	36
	1	21	141		1	29	150
	2	23	147		2	31	156
	3	16	21		3	24	30
	4	22	146		4	30	155
	5	20	140		5	28	149
	6	19	28		6	27	37
	7	17	22		7	25	31
U6	0	CB2	45	U8	0	34	87
	1	CB5	159		1	37	201
	2	CB7	165		2	39	207
	3	CB0	39		3	32	81
	4	CB6	164		4	38	206
	5	CB4	158		5	36	200
	6	CB3	46		6	35	88
	7	CB1	40		7	33	82
U9	0	42	96	U10	0	50	105
	1	45	210		1	53	219
	2	47	216		2	55	225
	3	40	90		3	48	99
	4	46	215		4	54	224
	5	44	209		5	52	218
	6	43	97		6	51	106
	7	41	91		7	49	100

**Table 7: Component-to-Module DQ Map (Continued)**

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	58	114	U13	0	61	228
	1	61	228		1	58	114
	2	63	234		2	56	108
	3	56	108		3	63	234
	4	62	233		4	57	109
	5	60	227		5	59	115
	6	59	115		6	60	227
	7	57	109		7	62	233
U14	0	53	219	U15	0	45	210
	1	50	105		1	42	96
	2	48	99		2	40	90
	3	55	225		3	47	216
	4	49	100		4	41	91
	5	51	106		5	43	97
	6	52	218		6	44	209
	7	54	224		7	46	215
U16	0	37	201	U17	0	CB5	159
	1	34	87		1	CB2	45
	2	32	81		2	CB0	39
	3	39	207		3	CB7	165
	4	33	82		4	CB1	40
	5	35	88		5	CB3	46
	6	36	200		6	CB4	158
	7	38	206		7	CB6	164
U18	0	29	150	U19	0	21	141
	1	26	36		1	18	27
	2	24	30		2	16	21
	3	31	156		3	23	147
	4	25	31		4	17	22
	5	27	37		5	19	28
	6	28	149		6	20	140
	7	30	155		7	22	146



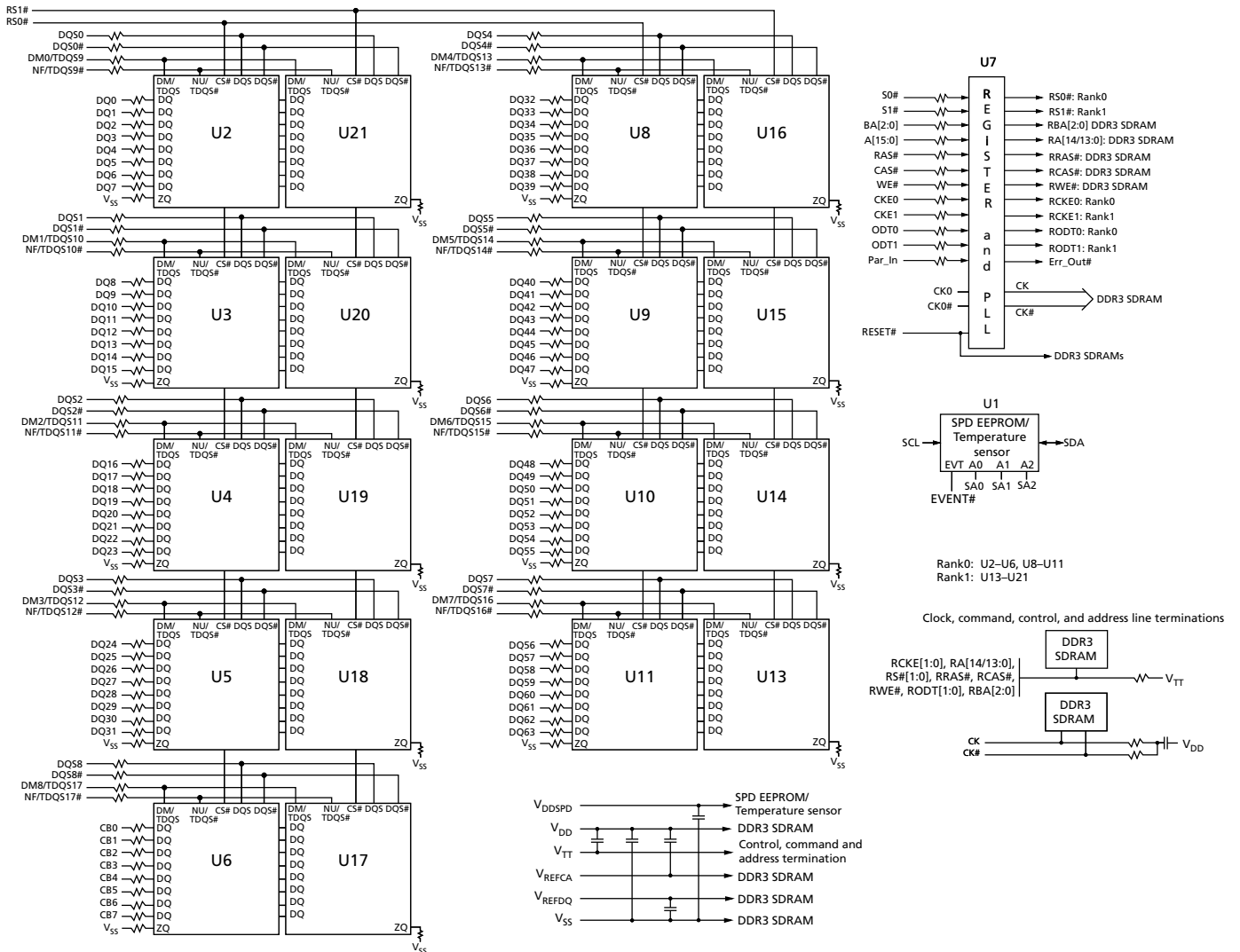
Table 7: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U20	0	13	132	U21	0	5	123
	1	10	18		1	2	9
	2	8	12		2	0	3
	3	15	138		3	7	129
	4	9	13		4	1	4
	5	11	19		5	3	10
	6	12	131		6	4	122
	7	14	137		7	6	128



## Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1 percent resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

## General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an  $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single  $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

## Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

## Registering Clock Driver Operation

Registered DDR3 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC standard "Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3 RDIMM Applications."

The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller.

## Parity Operations

The registering clock driver includes an even parity function for checking parity. The memory controller accepts a parity bit at the Par\_In input and compares it with the data received on A[15:0], BA[2:0], RAS#, CAS#, and WE#. Valid parity is defined as an even number of ones (1s) across the address and command inputs (A[15:0], BA[2:0], RAS#, CAS#, and WE#) combined with Par\_In. Parity errors are flagged on Err\_Out#.

Address and command parity is checked during all DRAM operations and during control word WRITE operations to the registering clock driver. For SDRAM operations, the address is still propagated to the SDRAM even when there is a parity error. When writing to the internal control words of the registering clock driver, the write will be ignored if parity is not valid. For this reason, systems must connect the Par\_In pins on the DIMM and provide correct parity when writing to the registering clock driver control word configuration registers.



## **Temperature Sensor with Serial Presence-Detect EEPROM**

### **Thermal Sensor Operations**

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I<sup>2</sup>C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

### **Serial Presence-Detect EEPROM Operation**

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I<sup>2</sup>C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V<sub>SS</sub>, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

## Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 8: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Units
$V_{DD}$	$V_{DD}$ supply voltage relative to $V_{SS}$	-0.4	1.975	V
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	-0.4	1.975	V

**Table 9: Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units	Notes	
$V_{DD}$	$V_{DD}$ supply voltage	1.425	1.5	1.575	V		
$I_{VT}$	Termination reference current from $V_{TT}$	-600	-	600	mA		
$V_{DD}$	Termination reference voltage (DC) – command/address bus	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V	1	
$I_I$	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$ ; $V_{REF}$ input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	-	-	-	$\mu\text{A}$	5
		DM	-4	0	4		
$I_{OZ}$	Output leakage current; $0V \leq V_{OUT} \leq V_{DD}$ ; DQ and ODT are disabled; ODT is HIGH	-10	0	10	$\mu\text{A}$		
$I_{VREF}$	$V_{REF}$ supply leakage current; $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)	-18	0	18	$\mu\text{A}$		
$T_A$	Module ambient operating temperature	0	-	70	$^{\circ}\text{C}$	2, 3	
$T_C$	DDR3 SDRAM component case operating temperature	0	-	95	$^{\circ}\text{C}$	2, 3, 4	

- Notes:
- $V_{TT}$  termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
  - $T_A$  and  $T_C$  are simultaneous requirements.
  - For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
  - The refresh rate is required to double when  $85^{\circ}\text{C} < T_C \leq 95^{\circ}\text{C}$ .
  - Inputs are terminated to  $V_{DD}/2$ . Input current is dependent on terminating resistance selected in register.



## DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's web site. Module speed grades correlate with component speed grades, as shown below.

**Table 10: Module and Component Speed Grades**

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G1	-093
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

## I<sub>DD</sub> Specifications

**Table 11: DDR3 I<sub>DD</sub> Specifications and Conditions – 2GB (Die Revision G)**

Values are for the MT41J128M8 DDR3 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter	Symbol	1866	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub> <sup>1</sup>	738	738	693	648	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub> <sup>1</sup>	918	918	873	828	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub> <sup>2</sup>	216	216	216	216	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub> <sup>2</sup>	630	540	540	450	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	810	720	630	630	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	900	810	720	630	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>2</sup>	648	603	558	513	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	630	630	540	540	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	900	810	720	720	mA
Burst read operating current	I <sub>DD4R</sub> <sup>1</sup>	1503	1368	1233	1053	mA
Burst write operating current	I <sub>DD4W</sub> <sup>1</sup>	1548	1413	1233	1098	mA
Refresh current	I <sub>DD5B</sub> <sup>1</sup>	1683	1638	1593	1548	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub> <sup>2</sup>	144	144	144	144	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub> <sup>2</sup>	180	180	180	180	mA
All banks interleaved read current	I <sub>DD7</sub> <sup>1</sup>	2448	2313	2223	1863	mA
Reset current	I <sub>DD8</sub> <sup>1</sup>	252	252	252	252	mA

- Notes: 1. One module rank in the active I<sub>DD</sub>, the other rank in I<sub>DD2P0</sub> (slow exit).  
2. All ranks in this I<sub>DD</sub> condition.

**Table 12: DDR3 I<sub>DD</sub> Specifications and Conditions – 4GB (Die Revision M)**

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1866	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub> <sup>1</sup>	783	738	693	648	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub> <sup>1</sup>	873	828	783	738	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub> <sup>2</sup>	216	216	216	216	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub> <sup>2</sup>	756	666	576	486	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	810	720	630	540	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	864	774	684	594	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>2</sup>	558	513	468	423	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	990	900	810	720	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	1080	990	90	810	mA
Burst read operating current	I <sub>DD4R</sub> <sup>1</sup>	1647	1512	1377	1278	mA
Burst write operating current	I <sub>DD4W</sub> <sup>1</sup>	1548	1413	1278	1143	mA
Refresh current	I <sub>DD5B</sub> <sup>1</sup>	1908	1863	1818	1773	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub> <sup>2</sup>	216	216	216	216	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub> <sup>2</sup>	243	243	243	243	mA
All banks interleaved read current	I <sub>DD7</sub> <sup>1</sup>	2403	2268	2133	1998	mA
Reset current	I <sub>DD8</sub> <sup>1</sup>	234	234	234	234	mA

- Notes: 1. One module rank in the active I<sub>DD</sub>, the other rank in I<sub>DD2P0</sub> (slow exit).  
2. All ranks in this I<sub>DD</sub> condition.



**Table 13: DDR3 I<sub>DD</sub> Specifications and Conditions – 4GB (Die Revision K)**

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb (256 Meg x 8) component data sheet

Parameter	Symbol	1866	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I <sub>DD0</sub> <sup>1</sup>	495	486	477	459	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I <sub>DD1</sub> <sup>1</sup>	630	612	594	558	mA
Precharge power-down current: Slow exit	I <sub>DD2P0</sub> <sup>2</sup>	216	216	216	216	mA
Precharge power-down current: Fast exit	I <sub>DD2P1</sub> <sup>2</sup>	270	270	270	270	mA
Precharge quiet standby current	I <sub>DD2Q</sub> <sup>2</sup>	396	396	396	396	mA
Precharge standby current	I <sub>DD2N</sub> <sup>2</sup>	414	414	414	414	mA
Precharge standby ODT current	I <sub>DD2NT</sub> <sup>2</sup>	432	414	396	396	mA
Active power-down current	I <sub>DD3P</sub> <sup>2</sup>	396	396	396	396	mA
Active standby current	I <sub>DD3N</sub> <sup>2</sup>	666	630	594	558	mA
Burst read operating current	I <sub>DD4R</sub> <sup>1</sup>	1098	1008	900	783	mA
Burst write operating current	I <sub>DD4W</sub> <sup>1</sup>	1134	1035	927	819	mA
Refresh current	I <sub>DD5B</sub> <sup>1</sup>	1764	1746	1737	1719	mA
Self refresh temperature current: MAX T <sub>C</sub> = 85°C	I <sub>DD6</sub> <sup>2</sup>	216	216	216	216	mA
Self refresh temperature current (SRT-enabled): MAX T <sub>C</sub> = 95°C	I <sub>DD6ET</sub> <sup>2</sup>	243	243	243	243	mA
All banks interleaved read current	I <sub>DD7</sub> <sup>1</sup>	1647	1575	1521	1260	mA
Reset current	I <sub>DD8</sub> <sup>1</sup>	234	234	234	234	mA

- Notes: 1. One module rank in the active I<sub>DD</sub>, the other rank in I<sub>DD2P0</sub> (slow exit).  
2. All ranks in this I<sub>DD</sub> condition.



## Registering Clock Driver Specifications

**Table 14: Registering Clock Driver Electrical Characteristics**

SSTE32882 devices or equivalent

Parameter	Symbol	Pins	Min	Nom	Max	Units
DC supply voltage	$V_{DD}$	–	1.425	1.5	1.575	V
DC reference voltage	$V_{REF}$	–	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V
DC termination voltage	$V_{TT}$	–	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V
AC high-level input voltage	$V_{IH(AC)}$	Control, command, address	$V_{REF} + 175\text{mV}$	–	$V_{DD} + 400\text{mV}$	V
AC low-level input voltage	$V_{IL(AC)}$	Control, command, address	–0.4	–	$V_{REF} - 175\text{mV}$	V
DC high-level input voltage	$V_{IH(DC)}$	Control, command, address	$V_{REF} + 100\text{mV}$	–	$V_{DD} + 0.4$	V
DC low-level input voltage	$V_{IL(DC)}$	Control, command, address	–0.4	–	$V_{REF} - 100\text{mV}$	V
High-level input voltage	$V_{IH(CMOS)}$	RESET#, MIRROR	$0.65 \times V_{DD}$	–	$V_{DD}$	V
Low-level input voltage	$V_{IL(CMOS)}$	RESET#, MIRROR	0	–	$0.35 \times V_{DD}$	V
Differential input crosspoint voltage range	$V_{IX(AC)}$	CK, CK#, FBIN, FBIN#	$0.5 \times V_{DD} - 175\text{mV}$	$0.5 \times V_{DD}$	$0.5 \times V_{DD} + 175\text{mV}$	V
Differential input voltage	$V_{ID(AC)}$	CK, CK#	350	–	$V_{DD} + \text{TBD}$	mV
High-level output current	$I_{OH}$	Err_Out#	–	–	TBD	mA
Low-level output current	$I_{OL}$	Err_Out#	TBD	–	TBD	mA

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of the DDR3 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module.



## Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I<sup>2</sup>C bus shared with the SPD EEPROM. Refer to JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

### Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: [www.micron.com/SPD](http://www.micron.com/SPD).

**Table 15: Temperature Sensor with SPD EEPROM Operating Conditions**

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V <sub>DDSPD</sub>	3.0	3.6	V
Supply current: V <sub>DD</sub> = 3.3V	I <sub>DD</sub>	–	2.0	mA
Input high voltage: Logic 1; SCL, SDA	V <sub>IH</sub>	V <sub>DDSPD</sub> × 0.7	V <sub>DDSPD</sub> + 1	V
Input low voltage: Logic 0; SCL, SDA	V <sub>IL</sub>	–0.5	V <sub>DDSPD</sub> × 0.3	V
Output low voltage: I <sub>OUT</sub> = 2.1mA	V <sub>OL</sub>	–	0.4	V
Input current	I <sub>IN</sub>	–5.0	5.0	μA
Temperature sensing range	–	–40	125	°C
Temperature sensor accuracy (class B)	–	–1.0	1.0	°C

**Table 16: Temperature Sensor and SPD EEPROM Serial Interface Timing**

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	t <sub>BUF</sub>	4.7	–	μs
SDA fall time	t <sub>F</sub>	20	300	ns
SDA rise time	t <sub>R</sub>	–	1000	ns
Data hold time	t <sub>HD:DAT</sub>	200	900	ns
Start condition hold time	t <sub>H:STA</sub>	4.0	–	μs
Clock HIGH period	t <sub>HIGH</sub>	4.0	50	μs
Clock LOW period	t <sub>LOW</sub>	4.7	–	μs
SCL clock frequency	t <sub>SCL</sub>	10	100	kHz
Data setup time	t <sub>SU:DAT</sub>	250	–	ns
Start condition setup time	t <sub>SU:STA</sub>	4.7	–	μs
Stop condition setup time	t <sub>SU:STO</sub>	4.0	–	μs

## **EVENT# Pin**

The temperature sensor also adds the EVENT# pin (open-drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

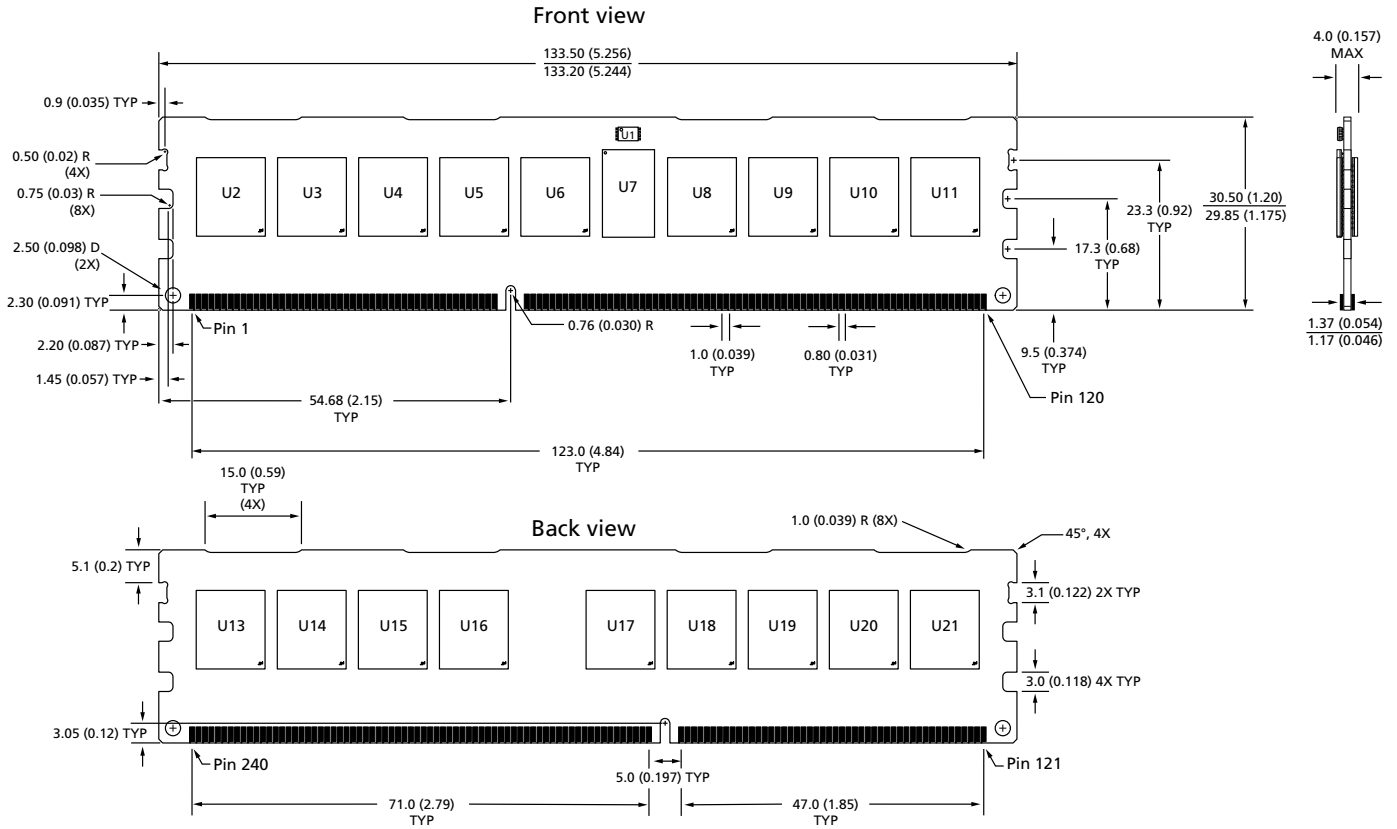
The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and returns to the logic HIGH state only when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

## Module Dimensions

**Figure 3: 240-Pin DDR3 RDIMM**



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.  
2. The dimensional diagram is for reference only.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.