PIC18F87J10 Family Rev. A2 Silicon Errata

The PIC18F87J10 family parts you have received conform functionally to the Device Data Sheet (DS39663**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F87J10 family will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F87J10 family devices with these Device/ Revision IDs:

Part Number	Device ID	Revision ID
PIC18F87J10	01 0111 011	00011
PIC18F86J15	01 0111 010	00011
PIC18F86J10	01 0111 001	00011
PIC18F85J15	01 0111 000	00011
PIC18F85J10	01 0101 111	00011
PIC18F67J10	01 0101 101	00011
PIC18F66J15	01 0101 100	00011
PIC18F66J10	01 0101 011	00011
PIC18F65J15	01 0101 010	00011
PIC18F65J10	01 0101 001	00011

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: ADC

When the A/D conversion clock is selected to be either FOSC/64, FOSC/32 or FOSC/16, the GO/DONE bit cannot be set for a second conversion without first selecting (temporarily) the RC oscillator as the A/D conversion clock. With the A/D conversion clock settings of FOSC/2, FOSC/4 and FRC, the A/D functions normally.

Work around

For A/D conversion clock settings of FOSC/64, FOSC/32 or FOSC/16, the following work around, shown in Example 1, must be performed prior to setting the GO/DONE bit for subsequent conversions.

It is recommended that this code be inserted immediately after the A/D result has been read from the previous conversion.

2. Module: ADC

When FOSC/8 is selected as the A/D conversion clock, A/D conversion will not be performed.

Work around

None.

EXAMPLE 1:

```
MOVF    ADCON2, W          ;copy the value of ADCON2 to WREG
BSF     ADCON2, ADCS0      ;temporarily select RC oscillator as clock
BSF     ADCON2, ADCS1
MOVWF   ADCON2             ;restore ADCON2 to original value
```

3. Module: MSSP

In SPI mode, the Buffer Full bit (BF in SSPxSTAT register), the Write Collision Detect bit (WCOL in SSPxCON1) and the Receive Overflow Indicator bit (SSPOV in SSPxCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in SSPxCON1 register).

For example, if SSPxBUF is full (BF bit is set) and the MSSP module is disabled, and then re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPxBUF will result in a write collision; or in SPI Slave mode, if a new byte is received, a receive overflow will occur.

Work around

Ensure that if the buffer is full, SSPxBUF is read (thus clearing the BF flag) before disabling the MSSP module. Also, ensure that WCOL is clear before disabling the MSSP module. If the module was configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

4. Module: MSSP

In its current implementation, the I^2C™ Master mode operates as follows:

a) The Baud Rate Generator for I^2C in Master mode is slower than the rates specified in Table 17-3 of the Device Data Sheet.

For this revision of silicon, use the values shown in Table 1 in place of those shown in Table 17-3 of the Device Data Sheet. The differences are shown in **bold** text.

b) Use the following formula in place of the one shown in Register 17-4 (SSPCON1) of the Device Data Sheet for bit description SSPM3:SSPM0 = `1000`.

SSPADD = INT((FCY/FSCL) – (FCY/1.111 MHz)) – 1

Note: The I^2C bus is a synchronous protocol, so the accuracy of the bus frequency is not critical.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: I^2C™ CLOCK RATE w/BRG

FOSC	FCY	FCY * 2	BRG Value	FSCL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	**0Eh**	400 kHz(1)
40 MHz	10 MHz	20 MHz	**15h**	312.5 kHz
40 MHz	10 MHz	20 MHz	**59h**	100 kHz
16 MHz	4 MHz	8 MHz	**05h**	400 kHz(1)
16 MHz	4 MHz	8 MHz	**08h**	308 kHz
16 MHz	4 MHz	8 MHz	**23h**	100 kHz
4 MHz	1 MHz	2 MHz	**01h**	333 kHz(1)
4 MHz	1 MHz	2 MHz	**08h**	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz(1)

Note 1: The I^2C™ interface does not conform to the 400 kHz I^2C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

5. Module: MSSP

After an I^2C transfer is initiated, the SSPxBUF register may be written for up to 10 TCY before additional writes are blocked. The data transfer may be corrupted if SSPxBUF is written during this time.

The WCOL bit is set any time an SSPxBUF write occurs during a transfer.

Work around

Avoid writing SSPxBUF until the data transfer is complete, indicated by the setting of the SSP1IF bit (PIR1<3>).

Verify the WCOL bit (SSPxCON1<7>) is clear after writing SSPxBUF to ensure any potential transfer in progress is not corrupted.

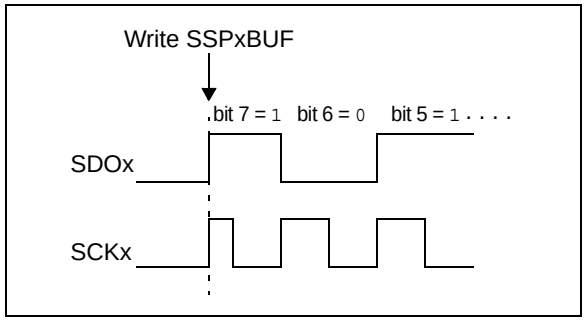
Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCKx pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCKx PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPxBUF with the data to transmit and then turn Timer2 back on. Refer to Example 2 for sample code.

EXAMPLE 2: AVOIDING THE INITIAL SHORT SCK1 PULSE (FOR MSSP1)

```
LOOP BTFSS  SSP1STAT, BF    ;Data received?
                            ;(Xmit complete?)
     BRA    LOOP            ;No
     MOVF   SSP1BUF, W      ;W = SSPBUF
     MOVWF  RXDATA          ;Save in user RAM
     MOVF   TXDATA, W       ;W = TXDATA
     BCF    T2CON, TMR2ON   ;Timer2 off
     CLRF   TMR2            ;Clear Timer2
     MOVWF  SSP1BUF         ;Xmit New data
     BSF    T2CON, TMR2ON   ;Timer2 on
```

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: MSSP

In SPI mode, the SDOx output may change after the inactive clock edge of the bit '0' output. This may affect some SPI components that read data over 300 ns after the inactive edge of SCKx.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: MSSP

It has been observed that following a Power-on Reset, I^2C modes may not initialize properly by just configuring the SCLx and SDAx pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

Work around

Before configuring the module for I^2C operation:

1. Configure the SCLx and SDAx pins as outputs by clearing their corresponding TRIS bits.
2. Force SCLx and SDAx low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCLx and SDAx as inputs by setting their TRIS bits.

Once this is done, use the SSPxCON1 and SSPxCON2 registers to configure the proper I^2C mode as before.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: MSSP

When the MSSP peripherals are configured for SPI mode, the Buffer Full bit, BF (SSPxSTAT<0>), should not be polled in software to determine when the transfer is complete.

Work around

Copy the SSPxSTAT register into a variable and perform the bit test on the variable. In Example 3, SSP1STAT is copied into the working register where the bit test is performed.

EXAMPLE 3: MSSP1

```
loop_MSB:
    MOVF   SSP1STAT, W
    BTFSS  WREG, BF
    BRA    loop_MSB
```

A second option is to poll the Master Synchronous Serial Port Interrupt Flag bit, SSP1IF (PIR1<3>). This bit can be polled and will set when the transfer is complete.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: A/D

The A/D offset is greater than the specified limit in Table 26-26 of the Device Data Sheet. The updated conditions and limits are shown in **bold** text in Table 2.

Work around

Three work arounds exist.

1. Configure the A/D to use the V_{REF}+ and V_{REF}- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed to 40 MHz and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 2: A/D CONVERTER CHARACTERISTICS: PIC18F87J10 FAMILY (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A06A	**E_{OFF}**	**Offset Error**	**—**	**—**	**<±5.0**	**LSb**	**V_{REF} = V_{REF}+ and V_{REF}-**
A06	E_{OFF}	Offset Error	—	—	**<±5.0**	LSb	**V_{REF} = V_{SS} and V_{DD}**

11. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the transmit buffer, TXREGx, are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREGx is written to;
- the baud rate counter overflows (at the end of the bit period); and
- a Stop bit is being transmitted (shifted out of TSR).

Work around

If possible, do not use the module's double-buffer capability. Instead, load the TXREGx register when the TRMT bit (TXSTAx<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, then load TXREGx immediately after TXxIF is set, or wait 1-bit time after TXxIF is set. Both solutions prevent writing TXREGx while a Stop bit is transmitted. Note that TXxIF is set at the beginning of the Stop bit transmission.

If transmission is intermittent, then do the following:

- Wait for the TRMT bit to be set before loading TXREGx.
- Alternatively, use a free timer resource to time the baud period. Set up the timer to overflow at the end of Stop bit, then start the timer when you load the TXREGx. Do not load the TXREGx when timer is about to overflow.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: EUSART

In 9-Bit Asynchronous Full-Duplex Receive mode, the received data may be corrupted if the TX9D bit (TXSTAx<0>) is not modified immediately after the RCIDL bit (BAUDCONx<6>) is set.

Work around

Write to TX9D only when a reception is not in progress (RCIDL = 1). Since there is no interrupt associated with RCIDL, it must be polled in software to determine when TX9D can be updated.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: EUSART

After the last received byte has been read from the EUSART receive buffer, RCREGx, the value is no longer valid for subsequent read operations.

Work around

The RCREGx register should only be read once for each byte received. After each byte is received from the EUSART, store the byte into a user variable. To determine when a byte is available to read from RCREGx, poll the RCIDL bit (BAUDCONx<6>) for a low-to-high transition, or use the EUSART Receive Interrupt Flag, RC1IF (PIR1<5>).

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: EUSART

With the auto-wake-up option enabled by setting the WUE bit (BAUDCONx<1>), the RC1IF (PIR1<5>) bit will become set on a high-to-low transition on the RXx pin. While the WUE bit is set, reading the receive buffer, RCREGx, will not clear the RCxIF interrupt flag. Therefore, the first opportunity to automatically clear RCxIF by reading RCREGx will happen only after WUE bit is cleared.

Note:	RCxIF can only be cleared by reading RCREGx

Work around

There are two workarounds available:

1. Poll the WUE bit and read RCREGx after the WUE bit is automatically cleared.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: Timer1

In 16-Bit Asynchronous Counter mode (with or without use of the Timer1 oscillator), the TMR1H and TMR3H buffers do not update when TMRxL is read.

This issue only affects reading the TMRxH registers. The timers increment and set the interrupt flags as expected. The timer registers can also be written as expected.

Work around

1. Use 8-bit mode by clearing the RD16 bit (T1CON<7>).
2. Use the internal clock synchronization option by clearing the T1SYNC bit (T1CON<2>).

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: CPU

The device current consumption is not reduced significantly when the device enters IDLE mode. The device does stop execution and peripherals continue to run as expected.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

17. Module: External Memory Bus

The A<19:16> EMB address lines and Read/Write control pins (OE, WRH and WRL) are released to their respective inactive states at the same time violating timing condition mentioned in Figure 26.5 and Figure 26.6 in the data sheet. This may result in peripheral device on the bus detecting an address change when Write/Read is initiated. The bus capacitance and signal delay on the address and control lines can affect the probability of invalid detection.

Work around

Two workarounds are available

1. Use a latch based on the falling edge of ALE to hold the A<19:16> signals.
2. Or, add a delay circuit to extend the valid time for A<19:16> signals to ensure the address is valid until Read/Write signals go inactive.

18. Module: External Memory Bus

For PIC18F8XXX devices, the Stack Pointer may incorrectly increment during a table read operation if the external memory bus wait states are enabled (i.e., Configuration bit, WAIT, is clear (CONFIG3L<7> = 0) and WAIT bits (MEMCON<5:4>) are not equal to '11').

Work around

If using the external memory bus and performing TBLRD operations with a non-zero wait state (CONFIG3L<7> = 0 and WAIT<1:0> (MEMCON<5:4>) are not equal to '11'), disable interrupts by clearing the GIE/GIEH (INTCON<7>) and PEIE/GIEL (INTCON<6>) bits prior to executing any TBLRD operation.

19. Module: Core (Program Memory Space)

Writes to program memory address 300000h, that are not blocked, can cause the program memory at different locations to be corrupted.

Work around

Do not write to address 300000h. If you wish to modify the contents of the Configuration registers, then modify the Configuration Words located at the end of the user memory (7FF4h for PIC18FX5J10 devices and 3FF4h for PIC18FX4J10 devices) and issue a Reset command. This will reload the Configuration registers with the new configuration setting.

REVISION HISTORY

Rev A Document (8/2005)
First revision of this document. Includes silicon issues 1 (ADC), 2 (ADC), and 3 (MSSP).

Rev B Document (5/2006)
Added silicon issues 4-9 (MSSP), 10 (A/D), 11-14 (EUSART), 15 (Timer1), 16 (CPU), 17 (External Memory Bus), 18, (External Memory Bus), and 19 (Core Program Memory Space).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona, Gresham, Oregon and Mountain View, California. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Alpharetta, GA
Tel: 770-640-0034
Fax: 770-640-0307

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

San Jose
Mountain View, CA
Tel: 650-215-1444
Fax: 650-961-0286

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8676-6200
Fax: 86-28-8676-6599

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7250
Fax: 86-29-8833-7256

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-5160-8631
Fax: 91-11-5160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Gumi
Tel: 82-54-473-4301
Fax: 82-54-473-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang
Tel: 60-4-646-8870
Fax: 60-4-646-5086

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

02/16/06