PIC16(L)F72X Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F72X family devices that you have received conform functionally to the current Device Data Sheet (DS41341**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F72X silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**AK**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F72X silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)						
		A7	A9	AA	AB	AC	AD	AK
PIC16F722	01 1000 100x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16LF722	01 1001 100x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16F723	01 1000 011x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16LF723	01 1001 011x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16F724	01 1000 010x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16LF724	01 1001 010x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16F726	01 1000 001x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16LF726	01 1001 001x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16F727	01 1000 000x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12
PIC16LF727	01 1001 000x xxxx	0x7	0x9	0xA	0xB	0xC	0xD	0x12

Note 1: The Device ID is located at 2006h. The five Least Significant bits comprise the revision ID.

2: Refer to the *"PIC16F72X Memory Programming Specification"* (DS41332) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)						
				A7	A9	AA	AB	AC	AD	AK
ADC (Analog-to-Digital Converter)	Power-down	1.1	ADC Power-down in Sleep.	X	X	X	X			
ADC (Analog-to-Digital Converter)	Offset Error	1.2	Error on Infrequent Conversions.	X	X	X	X	X		
ADC (Analog-to-Digital Converter)	Conversion Results	1.3	Incorrect Conversion below 0°C.	X	X	X	X	X		
Timer1	Timer1 Oscillator	2.1	Operation above 90°C.	X	X	X	X	X	X	X
Internal Oscillator	Frequency	3.1	Frequency Shift on Reset.	X						
Internal Oscillator	Frequency	3.2	Failure to wake from Sleep.	X	X					
Internal Oscillator	Frequency	3.3	Frequency Tolerance.	X	X	X	X	X	X	X
External Oscillator	External Oscillator	4.1	Operation below 2.7V in HS mode.	X	X	X	X	X	X	X
CPU	Sleep	5.1	Reset on Wake.	X	X					
BOR	Current	6.1	Current Draw in Sleep.	X	X	X	X			
WDT	`CLRWDT` Instruction	7.1	`CLRWDT` Instruction after WDT Time-out.	X	X	X	X	X		
Interrupts	Stack Push	8.1	Interrupt logic incorrectly pushes two addresses to the stack.	X	X	X	X	X	X	X
FVR	Initial Accuracy	9.1	Min. and Max. value change.							X

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (as applicable).

1. Module: ADC (Analog-to-Digital Converter)

1.1 ADC Power-down in Sleep

The ADC module incorrectly fails to power-down after a conversion if the device is in Sleep and the ADC interrupt is disabled. The proper operation is to power the ADC off after the conversion is complete if the device is sleeping and the ADC interrupt is disabled.

Work around

Use the ADC conversion complete interrupt (ADIF) to wake-up and explicitly shut down the ADC by clearing the ADON bit.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X				

1.2 Error on Infrequent Conversions

The offset error incorrectly exceeds the data sheet specifications if time between conversions is longer than 10 ms. If the time between conversions is greater than 10 ms, the offset error is 1 LSb typical and 3.3 LSb maximum.

Work around

The time dependent error is insignificant when the time between conversions is less than 10 ms. When the time between conversions is greater than 10 ms, take two back-to-back ADC conversions and discard the results of the first conversion.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X	X			

1.3 Incorrect Conversion below 0°C

In some devices, the ADC may improperly convert if the temperature is below 0°C and the ADC clock source is set to FOSC/8, FOSC/16, FOSC/32, FOSC/64.

Work around

Set the ADC clock source to FOSC/2, FOSC/4 or RC.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X	X			

2. Module: Timer1

2.1 Operation above 90°C

The Timer1 oscillator does not operate above 90°C.

Work around

None.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X	X	X	X	

3. Module: Internal Oscillator

3.1 Frequency Shift on Reset

The internal oscillator module may experience a ±1% frequency shift after a Reset. The frequency shift is not consistent and could cause the oscillator to operate outside of the 2% specification.

Work around

To minimize the chances of experiencing the frequency shift, the following steps should be taken:

1. Operate the internal oscillator at 8 MHz or 2 MHz.
2. Use an external pull-up on $\overline{\text{MCLR}}$ or use internal $\overline{\text{MCLR}}$ mode.
3. Disable the Power Reset Timer (PWRT).
4. The bypass capacitor and the Voltage Regulator Capacitor (VCAP) should be used appropriately to minimize noise in the device.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X							

3.2 Failure to Wake from Sleep

Due to internal race conditions upon entering Sleep mode, the device will occasionally fail to wake-up from Sleep. Only a device Power-on Reset will force the device to exit Sleep mode.

Work around

None. Do not use Sleep command.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X						

3.3 Frequency Tolerance

The frequency tolerance of the internal oscillator is ±2% from 0-60°C and ±3% from 60-85°C (see Figure 1).

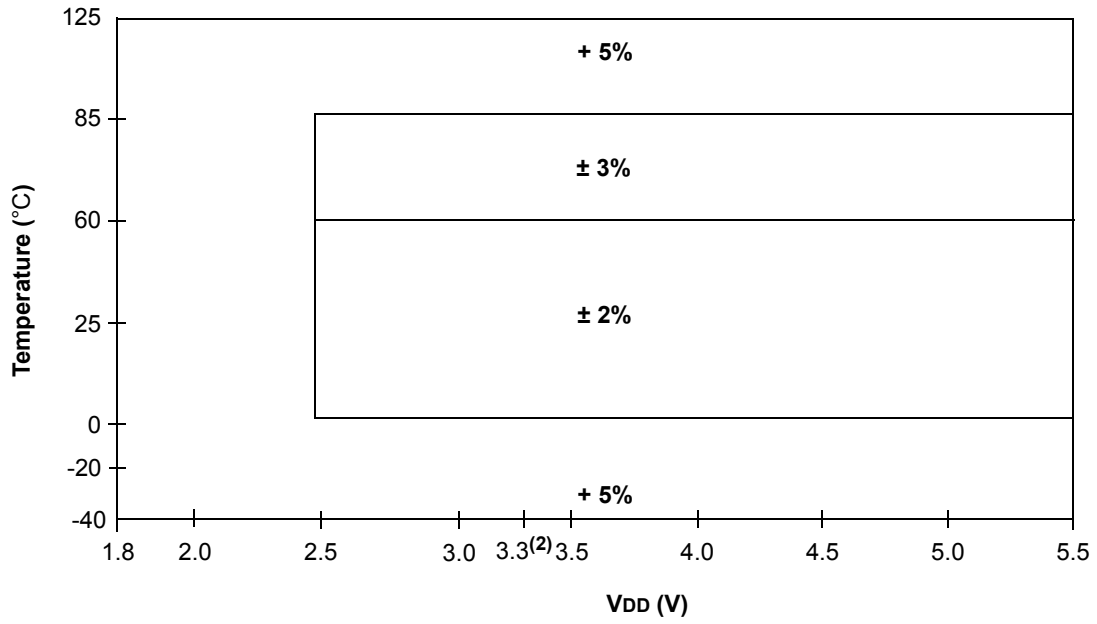
Work around

None.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X	X	X	X	

FIGURE 1: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE(1)



Note 1: This chart covers both regulator enabled and regulator disabled states.
2: Regulator Nominal voltage.

4. Module: External Oscillator

4.1 Minimum Operating Voltage for HS Mode

The minimum device VDD when using the external crystal oscillator in HS mode is 2.7V.

Work around

Use the internal oscillator or an external clock source if operation below 2.7V is required for the frequency range supported by HS mode.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X	X	X	X	

5. Module: CPU

5.1 Reset on Wake

If a wake from Sleep event occurs during the execution of a Sleep command, the device may reset. This Reset will be seen as a Power-on Reset to the device.

Work around

1. Disable all asynchronous interrupt before going to Sleep.
2. Make sure the timing of an asynchronous interrupt will not happen during the execution of the Sleep instruction.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X						

6. Module: BOR

6.1 Current Draw in Sleep

With the BOR set to “Enabled during operation and disabled during Sleep”, the device draws 2 μA more during Sleep than when the BOR is set to “Disabled”.

Work around

None.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X				

7. Module: WDT

7.1 CLRWDT Instruction after WDT Time-out

After a WDT Reset, the TO bit of the STATUS register remains clear until a SLEEP instruction or CLRWDT instruction is issued, then, the TO bit will be set. If the CLRWDT instruction is issued within 20 μS of the Reset, the TO bit will remain clear.

Work around

Wait at least 20 μS after a WDT Reset before using the CLRWDT instruction.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X	X			

8. Module: Interrupts

8.1 Stack Push

The interrupt logic incorrectly pushes two addresses to the stack when vectoring to the interrupt vector. Specifically, the interrupt vector address 0x4 is incorrectly pushed to the stack after the current PC, at the time the interrupt was received, is pushed. This will cause the stack to overflow if the user program is operating seven calls deep when an interrupt arrives. Because the stack is circular, the overflow causes the first stack address to be overwritten.

Work around

Disable interrupts by clearing the GIE bit in the INTCON register whenever the user program is operating seven calls deep. This ensures that interrupts will not cause the stack to overflow.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
X	X	X	X	X	X	X	

9. Module: FVR

9.1 Initial Accuracy

The initial accuracy values shown below in bold text have changed. These values are listed in the DC Characteristics Table 23-1, found in the Electrical Specifications chapter of the data sheet.

Work around

None.

Affected Silicon Revisions

A7	A9	AA	AB	AC	AD	AK	
						X	

D003	V_{FVR}	**Fixed Voltage Reference Voltage, Initial Accuracy**	**-8** **-8** **-8**	— — —	**6** **6** **6**	% % %	V_{FVR} = 1.024V, $V_{DD} \geq$ 2.5V V_{FVR} = 2.048V, $V_{DD} \geq$ 2.5V V_{FVR} = 4.096V, $V_{DD} \geq$ 4.75V; $-40 \leq T_A \leq 85°C$
			-8 **-8** **-8**	— — —	6 6 6	% % %	V_{FVR} = 1.024V, $V_{DD} \geq$ 2.5V V_{FVR} = 2.048V, $V_{DD} \geq$ 2.5V V_{FVR} = 4.096V, $V_{DD} \geq$ 4.75V; $-40 \leq T_A \leq 125°C$

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41341**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (07/2008)

First revision of this document.

Rev. B Document (08/2008)

Added Module 4: Internal Oscillator; Revised Modules 1 and 2.

Rev. C Document (11/2008)

Added Module 5: Internal Oscillator, Module 6: CPU and Module 7: BOR.

Rev. D Document (07/2009)

Updated document with new format. Added items 1.3 and 3.3. Updated Tables 1 and 2. Other minor changes.

Rev. E Document (09/2009)

Added Module 6: WDT; Revised Tables 1 and 2; Added Rev. ID AC.

Rev. F Document (01/2010)

Added Rev. AD Silicon.

Rev. G Document (03/2010)

Added new Module 4: External Oscillator; Revised Table 2; Revised Module 3.3: Frequency Tolerance; Other minor corrections.

Rev. H Document (04/2010)

Updated Tables 1 and 2, adding Rev. AK silicon; Updated Module 3, clarified condition.

Rev. J Document (02/2011)

Updated errata to new format; Added Module 8, Interrupts.

Rev. K Document (10/2013)

Updated errata to new format, Added Module 9, FVR; Other minor corrections.

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