PIC12(L)F1612/16(L)F1613

PIC12(L)F1612/16(L)F1613 Family Silicon Errata and Data Sheet Clarification

The PIC12(L)F1612/16(L)F1613 family devices that you have received conform functionally to the current Device Data Sheet (DS4001737**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC12(L)F1612/16(L)F1613 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC12(L)F1612/16(L)F1613 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1),(2)		
	DEV<8:0>	Revision ID for Silicon Revision	
		A0	A1
PIC16F1613	304Ch	0h	1h
PIC16LF1613	304Dh	0h	1h
PIC12F1612	3058h	0h	1h
PIC12LF1612	3059h	0h	1h

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC12(L)F1612/16(L)F1613 Memory Programming Specification"* (DS41720) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions (1)	
				A0	A1
TMR2	Interrupt	1.1	The TMR2, TMR4 and TMR6 modules may exhibit undesirable interrupt behavior when an ERS signal is used to Start/Stop the timer or in One-Shot mode.	X	
TMR2	One-Shot mode	1.2	Interrupt trigger can sometimes be lost in One-Shot modes.	X	
TMR2	Hardware Gate modes	1.3	Timer can continue to run after gated stop under certain circumstances if CKSYNC is not set.	X	
TMR2	One-Shot mode	1.4	Certain clock configurations can cause missed interrupt triggers in One-Shot modes.		X
CCP	PWM mode	2.1	The PWM mode will not be triggered as documented.	X	
CCP	PWM mode	2.2	With certain TMR2 settings, the PWM output will exhibit extra pulses.		X
CCP	Compare mode	2.3	Compare Toggle mode yields unexpected results.	X	X
ADC	Auto-trigger	3.1	The TMR2, TMR4 and TMR6 trigger inputs will not function as documented.	X	
ADC	Positive Voltage Reference	3.2	Using the FVR as the ADC positive voltage reference can cause missing codes.	X	X
CRC	Flash Memory Scan Trigger	4.1	The TMR2, TMR4 and TMR6 trigger inputs will not function as documented.	X	
SMT	Register Reset Values	5.1	SMT SFRs will only reset upon BOR and POR, not any other Reset sources.	X	X
FVR	ADC Conversion	6.1	First conversion of FVR signal may contain errors.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: TMR2

1.1 Interrupt

If the TMR2, TMR4, or TMR6 module is disabled or reset through an ERS signal or through One-Shot mode at the same time that it overflows, the interrupt will continue to set itself, even after being cleared.

Work around

The timer needs to be able to increment past the match case within the Interrupt Service Routine to clear the interrupt flag. Placing the following code in the ISR for the timer will alleviate the issue (see Example 1).

EXAMPLE 1: TIMER2 CONTINUOUS INTERRUPT WORK AROUND

```
banksel         TMR2
BCF             T2CON, T2ON; disable TMR to allow TMR2HLT settings changes
MOVFW           T2HLT; save off value of TMR2HLT
CLRF            T2HLT; clear off ERS state
BSF             T2CON, T2ON; pass the overflow state through to clear the interrupt
NOP             ; 1 cycle extra to clear the interrupt source (may not be needed)
BCF             T2CON, T2ON; disable TMR to allow TMR2HLT settings changes
MOVWF           T2HLT ; restore value of TMR2HLT
CLRF            TMR2 ; clear TMR2 to match rollover state before interrupt
BSF             T2CON, T2ON; re-enable TMR to match pre-interrupt state
```

Affected Silicon Revisions

A0	A1						
X							

1.2 One-Shot mode

In One-Shot mode, if the TMR2, TMR4 or TMR6 is reset through an external Reset signal at the same time the One-Shot mode disables the module through an overflow trigger, the interrupt will be “lost” and not properly triggered.

Work around

None.

Affected Silicon Revisions

A0	A1						
X							

1.3 Hardware Gate Modes

When the timer is operating in one of the hardware gate modes and the CKSYNC bit is clear, then an external gating event that stops and starts the timer at a timer value equal to or greater than the PR2 register will cause the timer to improperly continue to count beyond the PR2 period value.

Work around

Always set the CKSYNC bit when operating in the hardware gate modes.

Affected Silicon Revisions

A0	A1						
X							

1.4 One-Shot modes

For certain settings of PR2/PR4/PR6, CPU clock and Timer2/Timer4/Timer6 clock, the overflow interrupt for the Timer2 module will not trigger. In particular, this issue is most likely with a fast timer clock (TxCS not = to 000), a slow CPU clock, and a low-period value.

Work around

Restrict the values of PR2/PR4/PR6 according to the following equation:

EQUATION 1: TMRx PERIOD REGISTER RESTRICTIONS

$$PR_x > (F_{TMR\_clk}/F_{SYSTEM\_clk})*4–3$$

Where PRx is the period register value, F_{TMRx_clk} is the frequency of the input clock to the timer, and F_{SYSTEM_clk} is the frequency of the CPU clock.

Affected Silicon Revisions

A0	A1						
X	X						

2. Module: CCP

2.1 PWM mode

The PWM mode of the CCP will not be triggered as it is documented in the Timer2 chapter of the data sheet for Roll-Over modes.

Work around

The PWM mode of the CCP modules should not be used, except for Timer2 sourced by FOSC/4 in mode '0000'.

Affected Silicon Revisions

A0	A1						
X							

2.2 PWM mode

The PWM mode of the CCP may exhibit extra pulses/longer duty cycle with the Timer2 mode in any of the Edge-Triggered Hardware Limit modes (MODE<3:0> bits of TxCON = 0011, 0100 or 0101).

Under these settings, the following will occur:

For Timer2 Prescaler set to 1:1:

- If CCPW = 1, 2, or 3, the PWM will output a double pulse. In this case, the effective duty cycle is correct.
- If CCPW = >4, the PWM will output a single pulse, but the effective duty cycle will be DC+4.

For Timer2 prescaler set to 1:2:

- If CCPW = 1, the PWM will output a double pulse. In this case, the duty cycle will be correct.
- If CCPW = 2, the PWM will output a single pulse, but the effective duty cycle will be DC+4.

For Prescaler settings 1:4 or higher, there will only be a single pulse and the effective duty cycle of all CCPW settings will be DC+4.

Work around

If the extra duty cycle time or pulses would negatively affect the application, do not use the CCP with Timer2/4/6 configured in the affected modes.

Affected Silicon Revisions

A0	A1						
	X						

2.3. Compare Mode

The CCP Compare Toggle mode (CCP1M<3:0> bits = 0010) works properly as long as the Timer1 Prescaler value is configured to 1:1. When Timer1 prescaler value is configured to any other value, the ECCP Compare output yields unexpected results.

Work around

Only use the Compare Toggle mode when the Timer1 Prescaler value is set to 1:1.

Affected Silicon Revisions

A0	A1						
X	X						

3. Module: ADC

3.1 Auto-Trigger

The TMR2, TMR4 and TMR6 inputs for the automatic trigger of the ADC will exhibit incorrect behavior if the postscaler of the respective timer is anything other than 1:1, or if One-Shot mode is enabled.

Work around

Use only postscaler 1:1 in Roll-Over modes.

Affected Silicon Revisions

A0	A1						
X							

3.2. Positive Voltage Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Increase the bit conversion time, known as TAD, to 8 µs or higher.

Affected Silicon Revisions

A0	A1						
X	X						

4. Module: CRC

4.1 Flash Memory Scan Trigger

The TMR2, TMR4 and TMR6 trigger inputs will exhibit erroneous behavior if the postscaler of the respective timer is anything other than 1:1, or if the One-Shot mode is enabled.

Work around

Use only postscaler 1:1 in Roll-Over modes.

Affected Silicon Revisions

A0	A1						
X							

5. Module: SMT

5.1 Register Reset Values

SMT SFRs will only return to their documented Reset values upon a BOR or POR. For all other Reset sources, they will retain their previously held values.

Work around

After Reset, initialize any SMT SFRs that may have an effect on desired SMT function.

Affected Silicon Revisions

A0	A1						
X	X						

6. Module: FVR

6.1. ADC Conversion

When using the ADC to sample the output of the FVR, the first conversion result may contain errors. This can occur particularly if both the FVR and ADC modules have been powered down for significant time prior to the conversion.

Work around

Method 1:

Prior to the conversion, provide 'FVR Stabilization Period' per the graph provided in the Electrical Specification chapter of the data sheet. As shown in this graph, this stabilization time is typically in the range 25 to 30 µs. During this stabilization time, the ADC should be enabled and set the sample the VREFL (Vss) node. The following steps should be followed:

1. Enable ADC with sample path set to VREFL (Vss);
2. Enable FVR with ADFVR bits set to zero;
3. Configure FVR gain to the desired level per data sheet instructions;
4. Allow time for FVR stabilization. (Poll for FVRRDY = 1);
5. Configure ADC sample path to FVR and required ADC acquisition time allowed;
6. Initiate the ADC conversion

Method 2:

Alternately, the FVR and ADC modules can be enabled and a series of ADC conversions of the sampled FVR output performed while both modules remain active. In this case, the first conversion result should be discarded and the subsequent results utilized. It is noted that this approach, in effect, provides for the stabilization time referred to above.

Affected Silicon Revisions

A0	A1						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS4001737**C**):

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (02/2014)

Initial release of this document.

Rev B Document (06/2014)

Added Silicon Revision A1; Added 1.4 and 2.2 submodules; Added Module 6: WWDT, Other minor corrections.

Data Sheet Clarifications: Added Module 2.

Rev C Document (01/2017)

Added Modules 2.3, 3.2; Removed Module 6: WWDT; Added new Module 6: FVR.

Removed Data Sheet Clarifications (revised data sheet).

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